REMARKS

In the Office Action of January 4, 2006, the Examiner (1) objected to the title; (2) rejected claims 1, 2, 7-12, 25, and 25-32 under § 103(a) as being obvious over Chennupaty in view of Narayan; (3) rejected claims 3, 4, 13, 15, 16, and 27 under § 103(a) as being obvious over Chennupaty in view of Narayan and Google (New bytecodes for "real" Java?); (4) rejected claims 5, 6, 14, and 26 as obvious over Chennupaty in view of Narayan and JVM; (5) rejected claims 17-20 and 23-24 as obvious over Chennupaty in view of Narayan and Nazomi; (6) rejected claim 21 as obvious over Chennupaty/Narayan/Nazomi in view of Google; and (7) rejected claim 22 as obvious over Chennupaty/Narayan/Nazomi in view of JVM. In this Response, Applicants amend claims 1, 9, 17, and 25 and cancel claims 32-34.

Applicants submit a replacement version of paragraph [0001] of the specification to fill in the missing serial numbers. Applicants also submit a new Title as required by the Examiner.

Chennupaty discloses a decoder that is shown in a dashed box in Figure 3. The decoder shown includes three logic blocks including a prefix and escape detector 320 and an opcode decoder 340. Each instruction is represented by a number of bits. Some of the bits represent a prefix, if present. Some of the bits represent an escape code, if present. Some of the bits represent the opcode. In Figure 3, the prefix and escape code are represented by instruction bits designated as $I_N$ to $I_{N+7}$ and $I_K$ to $I_{K+7}$. See also col. 5. Instruction bits $I_M$ to $I_{M+7}$ represent the opcode. As can be seen in Figure 3, both the prefix and escape detector 320 and opcode decoder 340 receive the prefix and escape code bits.

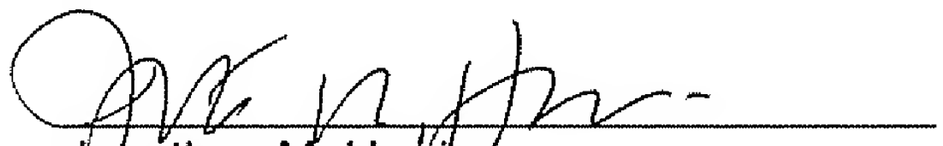
Claim 1 has been amended to clarify that, if the subsequent instruction includes the predetermined prefix, the program counter skips the prefix "thereby preclud[ing] decode logic from receiving the prefix." Chennupaty does not disclose this limitation. To the contrary, Chennupaty specifically teaches providing the prefix to the decoder.

No other art of record satisfies this deficiency of Chennupaty. Applicants note that the Examiner did not seem to be able to find a teaching in Chennupaty that the prefix is skipped as required in claim 1. See italicized paragraph on the Office Action's page 3, which is devoid of citations to Chennupaty. For at least this reason, claim 1 and all claims dependent thereon are allowable.

The same or similar amendment has been to independent claims 9, 17, and 25. For at least the same reason articulated above, claims 9, 17, and 25 and their dependent claims are in condition for allowance.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. Applicants hereby petition for any time extensions that are necessary to prevent this case from being abandoned. In the event that additional fees related to this Amendment, or other transactions in this case, are required (including fees for net addition of claims and for time extension), the Examiner is authorized to charge Texas Instruments Inc.'s Deposit Account No. 20-0668 for such fees.

Respectfully submitted,



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